

**VEECH ENGINEERING INCORPORATED**  
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**VEECH ENGINEERING INC.** is incorporated in the State of California since May 1991 and has \$1,000,000 liability insurance. Excellent REFERENCES/COMPLETED project folders available upon request.

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**ENGINEER:** Edward Witczak

BSEE, MSEE (all credits except thesis)  
30 Years Architecture/Analog/Digital/Firmware Design

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**PROJECT SCOPE:**

Electrical Engineering Design - Turn Key, Fixed Bid, T&M  
Corporate, Venture Capital - Technology Investigation and  
Presentations - FPGA Design - Wireless Systems

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**DESIGN SCOPE:**

ARCHITECTURE - System Architecture (SOC, Digital, Analog, RF)  
BOARD - Analog, Mixed Signal, and Digital Circuit Design  
LOGIC - High Speed (>1 GHz), FPGA (Xilinx, Altera, Cypress)  
EMBEDDED - 68XXX, 683XX, 68HCXX, 805X, TMSxxx, PIC, ARM  
LASER CONTROL - Control and Power Circuits  
SOC - Processor, Memory, Logic, and Sensor Interface  
INSTRUMENTATION - Specialized Test Equipment and Sensor Interface  
DSP HW - TMS320CXX, TMS320C6701, DSP96002, DSP56301, Others  
TELECOM - T1, E1, ADSL, Ethernet, Routing and Switching Systems  
RF, ZIGBEE - Hardware and Firmware Circuit Design and Interface  
HDL - Verilog, VHDL, AHDL (Altera), SPICE, CUPL  
FIRMWARE - C and Assembly (Motorola, Intel, PIC, ARM Processors)  
MIXED SIGNAL - Analog, ADC/DAC, SH Circuits, ISOAMPS, Sensors, RF  
MOTION CONTROL - Sync Phase Motors, Stepping Motors, Servo Motors, DC  
MEMORY USAGE - SRAM, DRAM, FPDAM, SDRAM, DSRAM, DDRAM, FIFO, FLASH  
INTERFACE - Ethernet, TCP/IP, VME Bus, PCI Bus, Custom, I2C  
SENSOR INTERFACE- Proximity, IR, Temperature, Pressure, Motion, Hall

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**DESIGN TOOLS PROFICIENCY:**

SCHEMATIC CAPTURE - Cadence OrCAD Capture and MENTOR GRAPHICS  
HDL COMPILERS/SYNTHESIS - XILINX-ISE Design Tools  
ALTEA-QUARTUS, MAX PLUS Design Tools  
CYPRESS-WARP Design Tools  
SYNPLICITY-Synplify Pro, Synthesis/Place/Route  
SYNOPSIS-FPGA Express, Synthesis/Place/Route  
HDL LANGUAGES - VERILOG, VERILOG 2001, VHDL, AHDL, PSPICE  
LOGIC SIMULATOR - MODEL TECHNOLOGY - ModelSim Verilog Simulator  
- MODEL TECHNOLOGY V-SYSTEM VHDL Simulator  
ANALOG SIMULATORS - MICRO-CAP PSPICE Simulator and Circuit Design  
C COMPILER - MICROSOFT, VARIOUS CROSS COMPILERS  
CAD - MATHCAD  
DEVELOPMENT SYSTEM - Various Device Dependent Development Systems  
LAB EQUIPMENT - Oscilloscopes, Spectrum & Logic Analyzers

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**PROJECT HISTORY:**

DOLBY LABS	SEP'08 -- JAN'09 ( 4 MONTHS)
VOLTERRA CORP.	AUG'08 -- SEP'08 ( 1 MONTHS)
RGA ASSEMBLY INC	MAR'08 -- AUG'08 ( 6 MONTHS)
VOLTERRA CORP.	MAR'07 -- FEB'08 (12 MONTHS)
AEROFLEX CORP.	JLY'07 -- DEC'07 ( 6 MONTHS)
VISTA POINT	AUG'07 -- SEP'07 ( 1 MONTHS)
CLEARWAVE SOFTWARE INC.	SEP'05 -- FEB'06 ( 6 MONTHS)
CANESTA CORPORATION	JUN'05 -- SEP'05 ( 4 MONTHS)
INTEL CORPORATION	JLY'04 -- APR'05 (10 MONTHS)
MASSIE RESEARCH LABS	JLY'03 -- DEC'03 ( 6 MONTHS)
DoD CONTRACT	MAR'03 -- JUN'03 ( 4 MONTHS)
EVANS ANALYTICAL GROUP	JLY'02 -- OCT'02 ( 4 MONTHS)
FIRST MEDICAL INC	JUN'01 -- MAR'02 (10 MONTHS)
RESEARCH PROJECT	FEB'01 -- JUN'01 ( 5 MONTHS)
COHERENT MEDICAL GROUP	OCT'00 -- JAN'01 ( 4 MONTHS)
APTIX SYSTEMS	AUG'00 -- OCT'00 ( 3 MONTHS)
KLA-TENCORE INC	MAR'00 -- JUN'00 ( 4 MONTHS)
SONIC SOLUTIONS INC	JUN'99 -- MAR'00 (10 MONTHS)
NIH RESEARCH GRANT	DEC'98 -- MAY'99 ( 6 MONTHS)
COHERENT MEDICAL GROUP	OCT'97 -- NOV'98 (14 MONTHS)
ULTRATECH STEPPER INC	APR'97 -- OCT'97 ( 7 MONTHS)
KLA INSTRUMENTS	JLY'95 -- SEP'96 (14 MONTHS)
AMATI COMMUNICATIONS CORP	JAN'95 -- MAY'95 ( 6 MONTHS)
MACROVISION INC	NOV'93 -- JAN'95 (15 MONTHS)
FUJITSU-ICL SYSTEMS	APR'93 -- SEP'93 ( 6 MONTHS)
COMPRESSION LABS INC	JUN'92 -- APR'93 (11 MONTHS)
DANTEC MEDICAL INC	FEB'91 -- OCT'91 ( 9 MONTHS)
SPECTRA PHYSICS INC	FEB'90 -- NOV'90 (10 MONTHS)
SINGER FLIGHT SIMULATION	MAR'89 -- FEB'90 (12 MONTHS)

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**SELECTED PROJECT DESCRIPTIONS:**

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**DOLBY LABS CORP.** - Analog Photo Sensor Circuit

Photo sensor circuit to detect the back light produced for a large screen LCD display system.

**VOLTERRA CORP.** - (SOC) Power Up Sequencer System-on-Chip

Follow-up work to System-on-Chip (SOC) hardware system architecture and logic development. System firmware architecture and code development. The system is used in Volterra's sequencer.

**RGA ASSEMBLY INC.** - RF Transmitter/Receiver Circuit, Handheld System

RF Transmitter/Receiver circuit to control a display panel. Design included the display panel and the hand held control unit. Carrier frequency was in the 915 MHz ISM band. The transmitter/receiver contained FSK transmitter/decoder circuits and a PIC processor.

The project contained the hardware, firmware, and mechanical design.

**VEECH ENGINEERING INC.** - NASA and NIH Grant Proposal

NASA RF(ISM Band) non-GPS location and tracking device grant proposal. NIH RF(ISM Band) non-GPS patient tracking device grant.

**VOLTERRA CORP.** - (SOC) Power Up Sequencer System-on-Chip

System-on-Chip (SOC) hardware system architecture and logic development. System firmware architecture and code development. The system is used in Volterra's power up sequencer.

The hardware consisted of SMBus instrument interface, embedded Flip8051 processor (50 MHz), boot program prom (1Kx8), internal data ram (1Kx8), and Flash Execution Prom (8Kx8) with various I/O logic. The total system and CRC check hardware was integrated on a chip and programmed in Verilog and C.

The hardware/firmware interfaced to various ADC's and DAC's as well as controlling various analog power circuits and implemented the SMBus standard.

The firmware consisted of a real time, multitasking architecture, interrupt driven, and controlled the chip functions, interfaced to the SMBus hardware, and performed various calculations. The firmware was programmed in C for the non-time sensitive tasks and assembly for the interrupt driven tasks.

The SMBus interface consisted of implementing the full standard set and CRC check. This was accomplished by a combination of hardware and firmware which interfaced to the 8051.

**AEROFLEX CORP.** - (SOC) High Security System-on-Chip Card Reader

System-on-Chip (SOC) hardware system architecture and logic development. The system consisted of a 8051 processor (48 MHz), Boot Prom (1kx8), Program Ram (32Kx8), 2kx8 SRam, 256x8 Dual Port Ram, USB Controller, and various I/O logic. Special SFR registers were mapped to provide various functional interfaces.

The system loaded a special "boot program" at power up from the Boot Prom and that program served as a loader for the USB Bus to download or change the stored program (in SRam). This operation could take place at power up or if needed when the system was operational.

The logic and interface hardware was programmed in Verilog.

**VISTA POINT** - Component evaluation. Analog circuit analysis and calculations.

- CLEARWAVE SOFTWARE INC.**
- 2.4GHz RF ZIGBEE 12/24VAC 4-CHANNEL POWER DRIVER
  - 2.4GHz RF ZIGBEE 110/220VAC 1-3 PHASE POWER DRIVER
  - 2.4GHz RF ZIGBEE TEMPERATURE SET, SENSE, AND DISPLAY

2.4GHz RF ZIGBEE ZIGBEE 12/24VAC 4-CHANNEL POWER DRIVER circuit interfaced with the ZIGBEE 2.4GHz RF transceiver (Chipcon CC2420) and is controlled by a PIC16F2620 processor. The 4 channels were capable of driving 12/24VAC at 4 AMPS/channel. The channels were controlled by dual SCR's and a zero cross (MOC3061-M) AC detector. The circuit had a sense circuit which detected the status of the AC line (on, off, error

detect). Power was supplied by one of the 12/24VAC lines, rectified, and regulated down to 3.3VDC to power the various devices.

2.4GHz RF ZIGBEE ZIGBEE 110/220VAC 3-CHANNEL POWER DRIVER circuit interfaced with the ZIGBEE 2.4GHz RF transceiver (Chipcon CC2420) and is controlled by a PIC16F2620 processor. The 3 channels were capable of driving 110/220VAC at 10 AMPS/channel. The channels were controlled by Triac's (MAC16CN) and a zero cross (MOC3061-M) AC detector. The circuit had a sense circuit which detected the status of the AC line (on, off, error detect). Power was supplied by one of the 110VAC lines, rectified, and regulated down to 3.3VDC to power the various devices. The circuit is capable of driving 3-110VAC, 1-220VAC and 1-110VAC, and 1-110/3 phase lines. Each phase is capable of driving 10 AMPS.

2.4GHz RF ZIGBEE TEMPERATURE SET, SENSE, AND DISPLAY circuit interfaced with the ZIGBEE 2.4GHz RF transceiver (Chipcon CC2420) and is controlled by a PIC16F2620 processor. The circuit operates from a 9V battery and is extremely low power (off state current consumption of <150 uA). The display consisted of a 3.5 digit LCD (Lumex LCD-S3X1C50TR/B). The circuit sensed and displayed the remote temperature, transmitted it over the Zigbee interface and was capable of setting a "target" temperature which regulated the ambient temperature.

#### **CANESTA CORPORATION** - 400MHz (2NS-6AMP/10NS-2AMP) PULSED CONSTANT CURRENT LASER DRIVER/CONTROL

Design consisted of a LVDS interface (LMH6533), 1.8GHz current feedback amplifier (THS3201), and 3.7GHz GaAs HJ-FET (NE6510179A) drivers. The circuit pulsed 6 AMPS for 2 NS (1ns rise/fall time) and superimposed this pulse on a 2 AMP 10ns pulse. The current feedback amplifier provided the constant current source feedback while the GasFET provided the drive. Both the 6 AMP (2NS) and the 2 AMP (10NS) pulse levels were remotely programmable from 0 to 7 AMPS) over a LVDS interface. The circuit was a controllable driver for a VCSEL LASER and L.E.D. array. The circuit drive pulses were capable and tested to a frequency of 300MHz constant current drive. The circuit was simulated in PSPICE, excellent matching to the actual circuit.

#### **INTEL CORPORATION** - FPGA DESIGN, ADVANCED PLATFORM DEVELOPMENT

Design consisted of a VERTEX-E, XCV400E BGA560 device to control the Advanced Platform Power, clock, and signal distribution logic. The I/O's consisted of mainly LVTTTL and GTL level signals. The input clock frequencies were 100MHz, 33MHz, and low frequency 33KHz for timer control. There was an extensive state machine (103 states) to control the cycling and all the output signals. The I/O's (123 total) were latched using synchronous SR latches. Approximately 40% of the I/O's were synchronized to the 33MHz clock. Signal routing multiplexers directed the I/O to various parts of the system.

The system controlled various peripherals which were part of the platform (PCIE Express, I2C Bus, various processor communications, DDRam Memory boards).

Complete simulation was done with MODEL TECHNOLOGY - ModelSim Verilog Simulator.

The code was implemented in Verilog 2001 with the use of ISE Design Tools and Synplify Pro, Synthesis, Place/Route tools. The approximate equivalent gate count was 95,000 gates.

**MASSIE RESEARCH LABS** - CURRENT and DATA CONTROL BOARD FOR LCD DISPLAY  
FPGA FOR PWM MULTIPLEXER AND CONTROL LOGIC  
FIRMWARE TO DRIVE SYSTEM

Current and Data Board: Controlled the LCD display current sources and data sent to the display. The data and control was over a PIC Processor parallel/serial port. Controlled RS422 communications ports. The current control was from D/A converters to drive constant current sources.  
Processor: PIC18F1220

FPGA Multiplexed EPLD: Multiplexed four PWM signals to any twelve (12) outputs. Logic and controlled for various functions of the system. Coded in Verilog. EPLD: Xilinx XCR3256XL

Complete simulation done with MODEL TECHNOLOGY - ModelSim Verilog Simulator.

Firmware: System and control code for the PIC18F8720 processor. The control consisted of driving 4 PWM channels to control 4 DC motors and 8 solenoids, driving 4 stepper motors and various other functions. Real time system driver allowed A/D, D/A, PWM of the stepper signals (4) allowing control of the count, period, and duty cycle. Coded in C.

**EVANS ANALYTIC GROUP** - Image Acquisition Board

The Image Acquisition Board received x,y, and z data from a wafer surface scan device, summed the data, performed data translation, and stored the data to SRam. When needed, data and coordinates were transferred to a host computer via a PCI Bus interface.

**FIRST MEDICAL INC** - STEP & SERVO CONTROL, LASER DRIVER, & PROCESSOR BOARD

The board controlled a blood analyzer system which detected proteins produced to detect heart attack victims. The board contained ten (10) stepping motors, servo spin motor controller, TMS320C31 DSP, seven RT thermistor interfaces, and a laser drive circuit. An Altera EPF10K50BC356 BGA FPGA was used for the system controller, stepping motor state machines, and a 1Kx8 Dual Port Ram. The board interfaced to an ISA bus for system commands.

**COHERENT MEDICAL GROUP** - 3 BOARD ANALOG/DIGITAL LASER CONTROL SYSTEM

Three board VME Laser Controller set. Boards consists of VME Interface, various digital I/O ports, RS232 interfaces. The boards contain two 32 channel analog multiplexers and two 16 bit A/D converters controlled by EPLDs to give a sample rate of 40 KHZ. There are three 16 bit and two 12 bit D/A converters. The incoming analog signals are received by differential receivers. Contains fiber driver & receivers for noisy environment and safety.

**ULTRATECH STEPPER INC** - PROCESSOR AND CONTROL BOARD

The board consists of a 68000 processor, 32x16 Flash Ram backup, 128kx16 Sram. Control signals and I/O ports controlled by EPLD's. Embedded test code for manufacture test.

**KLA INSTRUMENTS CORP** - 16 CHANNEL SCANNED VIDEO DEFECT ANALYZER BOARD

Fifteen channels of Reference, Test, and Defect 10 bit scanned video data is input to a pipeline consisting of a 2kx168 SyncFIFO, 2MEGx168 FP DRAM, and 256Kx168 SRAM. Defect reports (80 bits) come from another subsystem to a TMS320C50 processor which calculates the defect position in DRAM, determines if a defect is statistically needed for processing, and transfers a defect patch to SRAM. Once in SRAM, another TMS320C50 processor formats a header and multiplexes the defect data to a feature extraction subsystem. The board is 20"x12" and contains 240 chips. Three clocks control the system: 50 MHZ processing clock, 25 MHZ system clock, and 10 MHZ I/O clock. The system processes 8000 defects/channel.

**MACROVISION INC - VIDEO ENCODE, ENCRYPTION HARDWARE FIRMWARE SYSTEM**

The Video Encoder System takes NTSC and PAL video/audio signals and produces inverted horizontal vertical audio phase-crypt video scrambling Encrypted keys and data is sent via the video signal during vertical blanking. System used a 16MHZ 68306 uP with 2 Mwords DRAM. The system program and encryption algorithm is 32K of assembly language.

**COMPRESSION LABS INC - MPEG VIDEO COMPRESSION AND ENCODER BOARD**

The Video Compressor Board takes NTSC and PAL video/audio digitized data compresses and formats it to MPEG standard, and multiplexes the packetized data onto a bus. The board used a MC68302 for communications and control with 128kx16 Sram, 32kx16 Prom, and 256kx16 Flash. EPM7256, EPM7192, and EPM7096 EPLD'S are used for the packetization logic, (9) C-CUBE CL4000 compression chips with 1Mx16 DRAM each, and various FIFO's for data buffering. Three clocks are used: 80Mhz compression, 30Mhz chip communication, and 15Mhz system. NUBUS protocol processor communication. Board is 15"x15" containing 200 chips.

**AMATI COMMUNICATIONS CORPORATION - ADSL INTERFACE CARD**

The Asymmetric Digital Subscriber Line (ADSL) xmits data between the central office and a Linecard/POTS interface as follows: Fifteen RS422/T1/E1 simplex downstream channels, Fifteen downstream/upstream async/sync channels, and one low speed RS232 management channel (OAM). The T1/E1 interface uses LXT325 quad T1/E1 receivers. A FPGA muxes either T1/E1, RS422, or test data and performs B8ZS or HDB3 decoding.

**SPECTRA PHYSICS INC - 1 WATT Nd:YAG or Nd:YLF LASER CONTROLLER SYSTEM**

The Laser Controller consisted of 3 digital and 1 analog boards. The controller is a 8051 microprocessor with 2kx8 nonvolatile Ram and 32kx8 Prom. The analog board was a feedback control loop for the laser current drive. The system has a hand held remote unit, RS232 and GPIB capability. The system clock is 20Mhz with 100 chips.

**VERILINK INC (for PAC BELL D4 CHANNEL BANK) - T1 MULTIPLEXER FORMATTER**

The module consisted of 3 PCB's and is used to multiplex 6 T1 channels to a master channel residing in a D4 data bank. It consisted of 7 8051 uProcessors, a custom ASIC, (8kx8 PROM - 8kx8 NV Ram)/8051.

**COHERENT MEDICAL GROUP ----- ETHERNET, DRIVERS, WEB BROWSER INTERFACE**

**SONIC SOLUTIONS INC ----- DIGITAL AUDIO DVD MULTIPLEXER FIRMWARE**

**DANTEC MEDICAL INC ----- EEG MACHINE CONTROLLER**

**FUJITSU-ICL SYSTEMS ----- COMMUNICATIONS INTERFACE BOARDS**

**ARGO SYSTEMS INC ----- MULTI FREQUENCY SIGNAL MONITOR SYSTEM**

**SINGER FLIGHT SIMULATION INC -- 150 MHZ PIPELINE CLIPPING SIMULATOR BD**

**E.I.P. MICROWAVE INC ----- 250 MHZ PRESCAL COUNTER, YIG MIXER CTL**